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Applicant: Canon Inc.

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SPECIFICATION

1. TITLE OF THE INVENTION

Image Forming Processor

2. WHAT IS CLAIMED IS:

An image forming processor having digital circuitry and analog circuitry formed on a single chip in integrated fashion using a complementary metal-oxide semiconductor process structure, said digital circuitry comprising a microcomputer and peripherals of said microcomputer including a memory and a counter, said analog circuitry comprising operation amplifiers, comparators, and pulse width modulation circuits.

3. DETAILED DESCRIPTION OF THE INVENTION

[Industrial Field of Utilization]

The present invention relates to an image forming processor for use by image forming apparatuses such as copiers and printers.

[Prior Art]

Conventionally, image forming apparatuses such as copiers and printers have had their controlling and controlled circuits fabricated on completely separated

substrates. Typically, sequence controller circuits for controlling loads such as motors and solenoid valves and various power supplies for feeding low-voltage, exposure and charging power are furnished on substrates apart from those carrying these low-voltage, exposure, and charging power supply circuits.

In order to simplify such circuit arrangements, there has been proposed a method involving programs of a sequence control microcomputer providing stabilizing control over power supplies.

[Problem to be Solved by the Invention]

As mentioned above, conventional image forming apparatuses have had their controlling and controlled circuits built on separated substrates, so that it has been difficult to make these apparatuses smaller or more lightweight.

The proposed method for getting the workings of the power supplies stabilized using microcomputer programs has turned out to be costly and cumbersome. More specifically, the method involves initially measuring power supply output, converting the measurements from analog to digital form, inputting the digitized measurements into the microcomputer for program control, and subjecting the outcome of the program control to

pulse width modulation (PWM) control. To obtain high-speed response, high-precision output with this method requires installing a high-speed microcomputer and a highly accurate A/D converter. This can be an expensive practice fraught with programming complexities. Furthermore, peripheral circuits of the microcomputer, i.e., analog circuits such as driver circuits and level conversion circuits, still remain as discrete circuits. This does not contribute to making the entire setup as small and simple as desired. The proposal, despite its advantages, has thus failed to be materialized on a commercial basis.

The present invention has been made in view of the above circumstances and provides an image forming processor designed to make an image forming apparatus incorporating the processor smaller in size and less expensive than before.

[Means for Solving the Problem]

In achieving the foregoing and other objects of the present invention and according to one aspect thereof, there is provided an image processing processor having digital circuitry and analog circuitry formed on a single chip in integrated fashion using a complementary metal-oxide semiconductor (C-MOS) process structure, the

digital circuitry including a microcomputer and peripherals of the microcomputer including a memory and a counter, the analog circuitry including operation amplifiers, comparators, and pulse width modulation (PWM) circuits.

[Function]

With the above structure in place, the controlling circuits of the image forming apparatus hosting the processor are made smaller in size and consume less power than before.

[Preferred Embodiment]

One preferred embodiment of this invention will now be described. Fig. 1 is a block diagram of an image forming processor practiced as one embodiment of this invention. Fig. 2 is a circuit diagram of a switching regulator connected to the image forming processor.

In Fig. 1, what is enclosed by dashed lines constitutes a one-chip image forming processor. In Fig. 1, reference character Q1 denotes a CPU core that includes a memory and an internal bus.

Q2 through Q11 stand for operation amplifiers or comparators; Q12 and Q13 for analog multiplexer circuits; Q14 through Q16 for PWM (pulse width modulation) circuits; and Q17 and Q18 for timer counters. Q19 stands

for an LCD driver, Q20 for a control circuit that controls communication with an external device, Q21 for a CPU reset circuit activated upon power-up, Q22 for a watchdog timer circuit for detecting a program runaway on the CPU, and Q23 for a constant-voltage power supply.

The comparator Q2, together with transistors Tr5 and Tr6 as well as devices L1 and C10 furnished outside the chip, constitutes an automated switching power supply that supplies power (+5V) to this chip. The voltage supplied to this circuit comes from the switching regulator circuit shown in Fig. 2. Part of the supplied power is applied to the constant-voltage power supply Q23 via a resistor R4. The comparator Q2 compares a reference voltage from the power supply Q23 with a 5V output appearing on the point where the devices L1 and C10 are connected, in order to stabilize the 5V output by varying the current-carrying capacity of the transistor Tr6. This output is provided as a bias power supply within the chip covering the power supply for the CPU core Q1 as well.

The reset circuit Q21 detects the timing of leading edges of the 5V power supply so as to feed reset pulses to the CPU core Q1. The watchdog timer Q22 detects an abnormal state of repeat signals stemming from programming, and causes the reset circuit Q21 to generate

reset pulses accordingly. The operation amplifier Q3 is used as a differential amplifier for effecting stabilizing control over a 24V power supply that is fed to drive devices such as motors and solenoid valves as well as to the power supplies for exposure, charging, developing, and transcription. The operation amplifier Q3 compares the output of the constant-voltage power supply Q23 with a rectified smoothed output of a 24V winding in a converter transformer T21 as part of the switching regulator in Fig. 2. The result of the comparison is used as the basis for controlling a photodiode current of a photo-coupler Pc1. As illustrated in Fig. 1, various motors and solenoid valves are connected to output ports. Outputs of numerous sensors connected to input ports are detected by the CPU and forwarded to the output ports in keeping with procedures recorded beforehand in a program memory of the CPU, whereby the connected motors and solenoid valves are controlled.

In case of a sensor output error, a field-effect transistor (FET) Tr1 connected to an input terminal of the operation amplifier Q3 is turned on to bring the 24V power supply to zero volt, thus deactivating all motors and solenoid valves as well as the exposure, charging and developing power supplies. If an abnormal temperature

rise or an operational failure of a fusing heater or an exposure lamp is detected, field-effect transistors (FET) Tr3 and Tr4 are turned on to charge an external capacitor C9. This arrangement makes it possible to sustain error detection mode at least for a predetermined time period even after the line power is turned off.

The comparator Q4, operation amplifier Q5, and FET Tr4 constitute an A/D converter placed under control of the CPU. The A/D converter is used as part of a setup for detecting: the set voltage of a density adjusting variable resistor VR1 selected by a multiplexer; the voltage of a temperature-detecting thermistor of a fusing roller; and the output of a photodiode Pc2 for fluorescent lamp light volume control.

The timer counter Q17 constitutes a D/A converter subject to control of the CPU. The output of the timer counter Q17 is switched by the multiplexer Q13, which makes it possible to put the PWM circuits Q14 through Q16 under program control of the CPU. That is, the fluorescent lamp light volume, a high-voltage for charging, and a developing bias DC voltage are subjected to program control of the CPU.

The timer counter Q18 generates a developing bias AC signal also subject to program control by the CPU. The

LCD driver Q19 controls an LCD indicator connected externally. The serial I/O Q20 carries out communications with external devices such as checkers for adjustment and verification used at the factory or on the market, as well as application devices including ADF, DF, and sheet counters.

Referring to Fig. 2, a regulator circuit 103 provides PWM control over a switching FET Tr101 with signals having undergone optical conversion by the photodiode Pc1. This arrangement stabilizes the 24V output on the secondary side of the converter transformer T21.

Fig. 3 is a circuit diagram of an operation amplifier built with a C-MOS process structure.

In Fig. 3, FET's Q201, Q202, Q206, Q207, and Q209 are P-channel metal oxide semiconductors (PMOS); and FET's Q203, Q204, Q205, and Q208 are N-channel metal oxide semiconductors (NMOS). The input FET's Q201 and Q202 and the FET's Q203 and Q204 make up a differential amplifier. The FET's Q206, Q207, and Q209 constitute a constant-voltage power supply. The FET's Q205 and Q208 compose an amplifier, while C200 denotes a phase compensating capacitor.

The structure described above or its variations are

used to constitute the analog circuits such as comparators and PWM circuits.

The digital circuits such as the microcomputer and its peripherals including memories and counters are formed in increments of an arrangement wherein the drain of an NMOS FET and that of a PMOS FET are interconnected.

The image forming processor, structured as described above, is capable of handling all aspects of control: detection of the output from various sensors such as switches and photo interrupters; control over driving devices such as monitors, solenoid valves and relays based on the detected sensor output; control over the power supplies for sequence control and those for providing low-voltage, exposure, charging, and developing power; and control over LED and LCD displays.

The image forming processor of this invention may alternatively be built using a silicon gate CMOS process structure with its power supply voltage set approximately for 5V or less.

The image forming processor of the invention may be equipped with a power-saving mode feature. More specifically, if input is not made through a particular port for a predetermined period of time after a copying process, the processor may enter power-saving mode by

lowering the clock frequency of its CPU Q1. Later, when input is made through the port in question, the processor may return to its normal operation mode.

[Effects of the Invention]

As described, the image forming processor according to this invention offers the following major benefits:

(a) With most of the controlling circuits such as sequence controllers and power supply control circuits concentrated in a single-chip image forming processor, it is easy to build a small-sized image forming apparatus such as a copier or a printer incorporating the processor.

(b) The CPU is freed from the task of effecting power supply stabilizing control that is taken over by analog circuits. That means a low-cost CPU can be adopted by the inventive processor.

(c) The entire image forming processor chip can be structured using C-MOS's. That means no special manufacturing process is needed and that the chip is made smaller in size with lower levels of power dissipation than before.

4. BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an image forming processor practiced as one embodiment of this invention;

Fig. 2 is a circuit diagram of a switching regulator connected to the embodiment; and

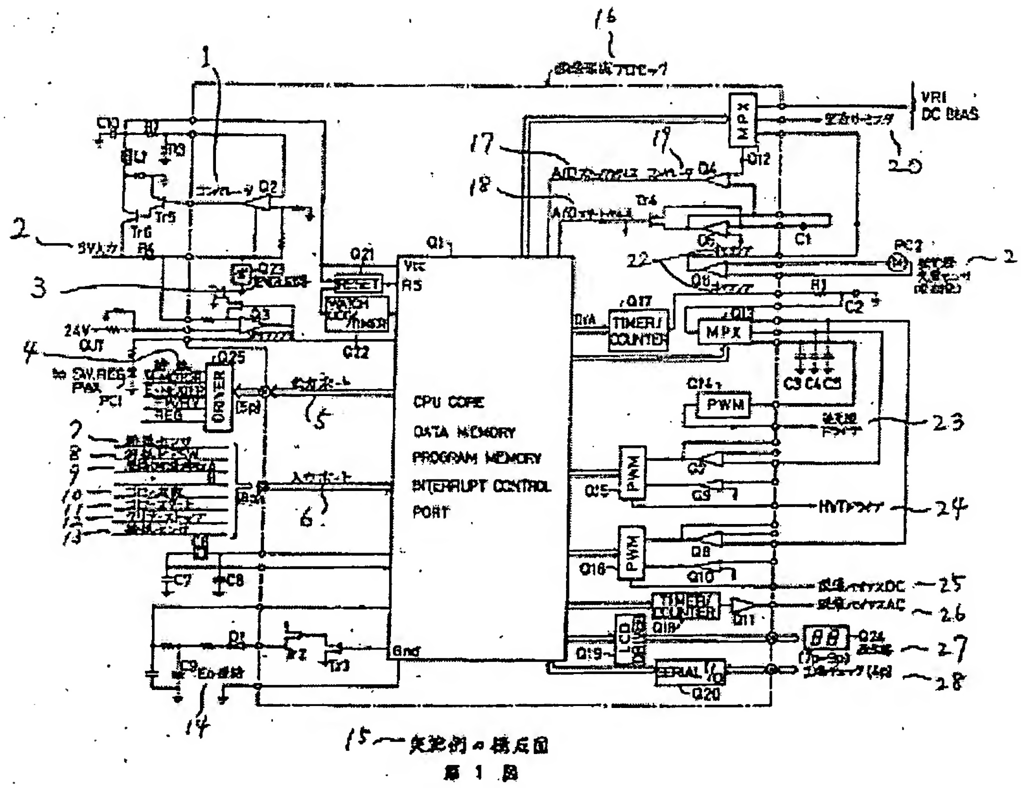
Fig. 3 is a circuit diagram of a C-MOS operation amplifier for use with the embodiment.

Q1 ... CPU core

Q2 to Q11 ... operation amplifiers or comparators

Q14, Q15, Q16 ... PWM circuits

FIG. 1



1: COMPARATOR

2: 5V INPUT

3: CONSTANT-VOLTAGE CIRCUIT

4: SHEET FEED

5: OUTPUT PORT

6: INPUT PORT

7: SHEET DELIVERY SENSOR

8: SHEET DELIVERY DOOR SWITCH

9: DOCUMENT FEEDER POSITION SENSOR A

10: COPY COUNT

11: COPY START

12: CLEAR/STOP

13: SHEET FEED SENSOR

14: EO HOLD

15: BLOCK DIAGRAM OF THE EMBODIMENT

16: IMAGE FORMING PROCESSOR

17: A/D STOP PULSE

18: A/D START PULSE

19: COMPARATOR

20: FUSING THERMISTOR

21: FLUORESCENT LAMP LIGHT VOLUME SENSOR (TO BE ADJUSTED)

22: OPERATION AMPLIFIER

23: FLUORESCENT LAMP DRIVE

24: HVT DRIVE

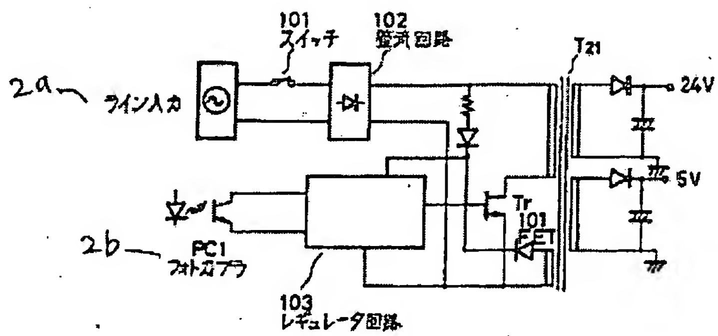
25: DEVELOPING BIAS DC

26: DEVELOPING BIAS AC

27: INDICATOR

28: FOR CHECKS AT FACTORY (4P)

FIG. 2



実施例で用いられるスイッチングレギュレータの回路図
第 2 図

CIRCUIT DIAGRAM OF SWITCHING REGULATOR

USED IN THE EMBODIMENT

2a: LINE INPUT

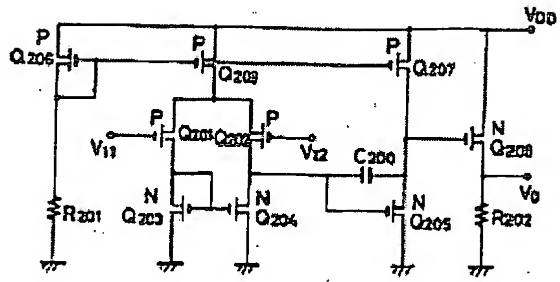
101: SWITCH

102: RECTIFIER CIRCUIT

2b: PC1 PHOTO-COUPLER

103: REGULATOR CIRCUIT

FIG. 3



実施例で用いるC-MOSのオペアンプの回路図

第 3 図

CIRCUIT DIAGRAM OF C-MOS OPERATION AMPLIFIER USED IN THE EMBODIMENT